Whitepaper: PCI-X – Narrowing the Performance Gap Between the Processors and the I/O Devices

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Need for Higher Performance I/O Technology

The global proliferation of the Internet has set a stage for people to demand new things from the Network – realistic information in realtime, independent of time and place. Overall infrastructure has been adapting to meet this requirement at various levels by developing new standards and technologies. At the heart of the development are new standards for higher performance I/O to meet the growing requirement for more bandwidth and higher throughput. WAN is transforming from T1/T3 to OC192 capable of supporting 1024MBytes/sec. 10BaseT Ethernet is rapidly becoming obsolete by the introduction of Gigabit Ethernet supporting up to 1024Mbit/sec. SCSI and Fiber Channel for storage interconnection are migrating from 80MBytes/sec SCSI to dual channel Ultra320 capable of operating at 640MBytes/sec, and 1GHz Fiber Channel to dual channel 2GHz Fiber Channel supporting up to 800MBytes/sec.

The other significant development in meeting the demands of people is the rapid increase of performance in microprocessors. The processor speed has increased 800% from 60MHz in 1992 to 450MHz in 1998. As a result, the processor can process more data, requiring more data to be available faster at the processor bus. In addition, the technological advancements in IC manufacturing allow highly specialized functions to be integrated into the processors. Thus, low cost application-specific systems are possible. Along with faster processors and application specific processors, these high performance I/O technologies provide a foundation for the emerging distributed processing systems in the network infrastructure.

The overall result of these developments is more data movement within the network infrastructure. This in turn, places a heavy burden on interconnect technology between the processors and the I/O devices within the intelligent I/O subsystem to support significantly higher data rates.

Up to now PCI bus technology has played a significant role in bridging the processors with fast I/O device in a cost-effective manner, leveraging the economies of scale provided by the PC market. However, as more high performance devices share the common I/O bus, requesting higher quality information faster to feed various subsystems in the network, PCI technology is rapidly reaching its upper performance limit. Figure 1 demonstrates one of many ways of representing the growing performance gap between the processor and the I/O speeds.

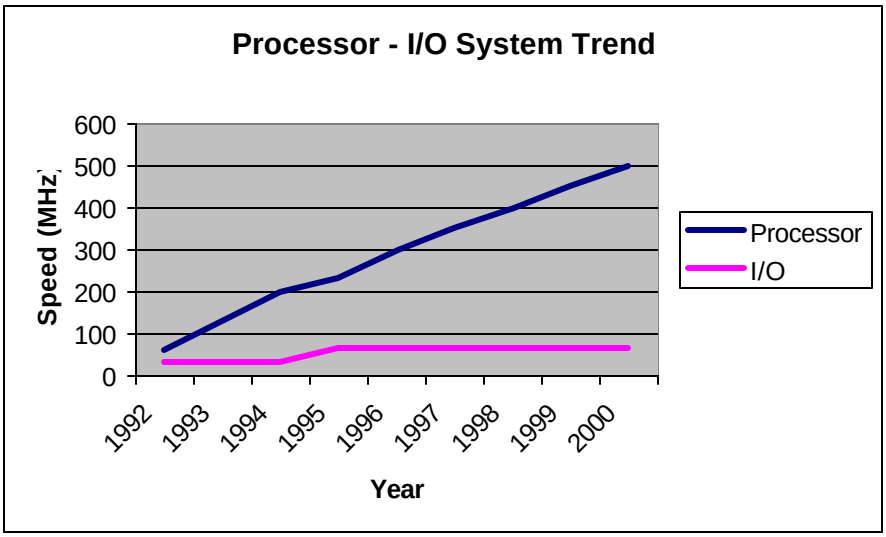

Figure 1: Comparison of Processor and I/O System speeds

However, even the latest PCI Local Bus Specification Revision 2.2 with 64-bit, 66MHz interface boasting 528MBytes/sec throughput, poses imbalance between the processor and I/O performance. With constant advancements in I/O devices, such as SCSI, Fiber Channel, Gigabit Ethernet, and multi-port Network Interface controller products, the demand for the next generation high performance I/O bus, which provides a simple migration from the current PCI technology, is at a critical stage. The core requirements for this new technology are that it must protect the current investment, while providing a higher bandwidth, lower latency, and higher slot capacity than the current PCI bus.

PCI-X: An Evolutionary Migration Path for PCI

To address this growing requirement, an enhancement to the PCI bus was introduced. PCI-X provides an evolutionary path that allows a higher bandwidth, an increased expansion slot capacity, and an industry standard bus that is backward compatible with the current PCI bus. PCI-X doubles the critically required bandwidth from 528MB/s to 1064MB/s to provide a greater I/O performance at the board level. Other benefits of PCI-X include: additional slot support at 66MHz (up to 4 slots) and 66MHz PCI-X system which is simpler to design than a 66MHz PCI system. Figure 2 illustrates PCI-X's capability in meeting today's higher bandwidth requirements for various I/O technologies.

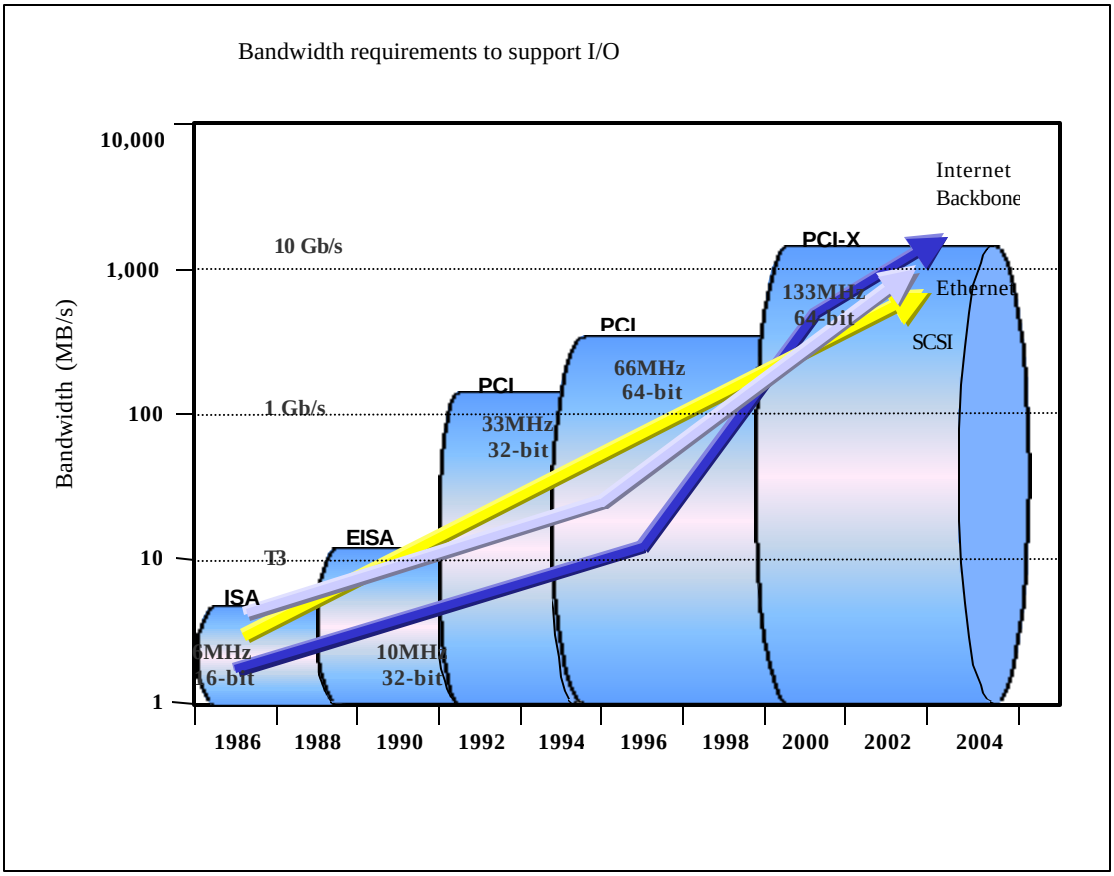

Figure 2: Bandwidth requirements to support I/O

The PCI-X introduces several major enhancements that enable faster and more efficient data transfers:

- Higher frequencies up to133MHz – doubling the performance achieved by the conventional PCI operating at 66MHz.
- Signal protocol changes to enable registered outputs and inputs – providing more relaxed requirement on timing, which eases the design.
- New information passed with each transaction enabling more efficient buffer management schemes. Resulting in improving bus bandwidth utilization.
- Restricted wait state and disconnection rules optimized for more efficient use of the bus and memory resources.
- Delayed Transactions in conventional PCI replaced by Split Transactions in PCI-X – further simplifying the design and increasing the overall performance.
- A wider range of error recovery implementations for PCI-X devices reducing system intervention on data parity errors.

Figure 3 provides a comparison of PCI-X to PCI.

Feature	*PCI*	*PCI-X*
PCI slot compatibility	Yes	Yes
100MHz Bus Speed	No	Yes
133MHz Bus Speed	No	Yes
Data Bus Width	32/64-bit	32/64-bit
Address Bus Width	32/64-bit	64-bit
Max Bus Bandwidth	533MBytes/sec	1064MBytes/sec
Multiple Slot support	Yes	Yes
Hierarchical bus topology	Yes	Yes
Split transactions	Open	Yes
Transaction Byte Count	No	4K
Non-coherent transactions	No	Yes
No/Relax Ordering rules	No	Yes
Device & Bus # ID	No	Yes

Figure 3: Comparison of PCI-X to PCI

Enabling PCI-X Applications

For any new technology to be widely adopted in the industry, there needs to be building blocks to enable the technology, including a standard, software, development tools, and finally, integrated circuits. An open standard is an important criteria for acceptance and utilization in the industry. For this requirement there is already a standard for PCI-X from PCISIG. Compaq, IBM, and HP, along with other major companies, played a vital role in making PCI-X a standard. Compaq, as an enabling leader, is setting up the building blocks necessary for the success of the technology by providing a proven PCI-X core, and by attracting and committing various semiconductor and system vendors to develop key products in implementation PCI-X-based products and systems. The key building blocks of enabling PCI-X acceptance include host PCI-X bridges, fast I/O devices, such as SCSI and Fiber Channel devices, PCI/PCI-X bridges, PCI-X cores, and eventually processors with integrated host PCI-X bus. Currently, a number of companies are developing these products, which will be introduced in the second half of 2000. Initial adoption will occur in the high performance server and storage applications to bridge the I/O performance gap between the storage subsystem and the main processor.

As the PCI-X becomes the main stream interconnect technology, embedded applications will begin to adopt the technology, including networking and communications market segments. A trend that was evident in adoption of PCI in the embedded market will occur with the PCI-X, but at a faster rate since it is an evolutionary change from PCI. These variations of PCI-X devices allow simple and cost-effective implementation of systems in the server/storage, networking, and telecommunication applications.

Figure 4 and Figure 5 are typical applications that leverage the new PCI-X technology.

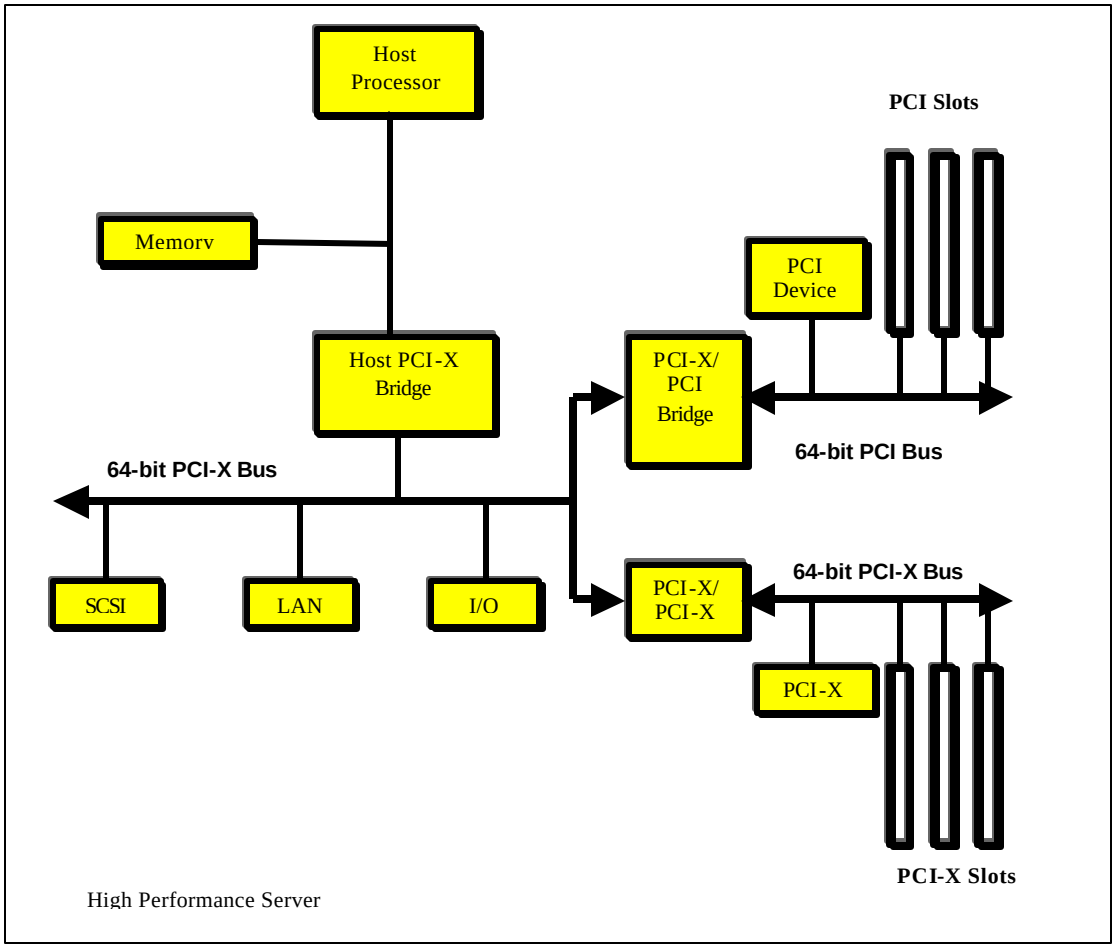

Figure 4: Typical Application – High Performance Server

In this high performance server application, a host PCI-X Bridge provides the bandwidth required to feed the high performance CPU from various high-speed I/O peripherals. At 66MHz, up to four high performance PCI-X devices can share this host PCI-X bus. Additional PCI-X-to-PCI-X bridges can extend the PCI-X/PCI slot or device capacity on the host PCI-X bus, as well as isolating the slower PCI bus from the PCI-X bus.

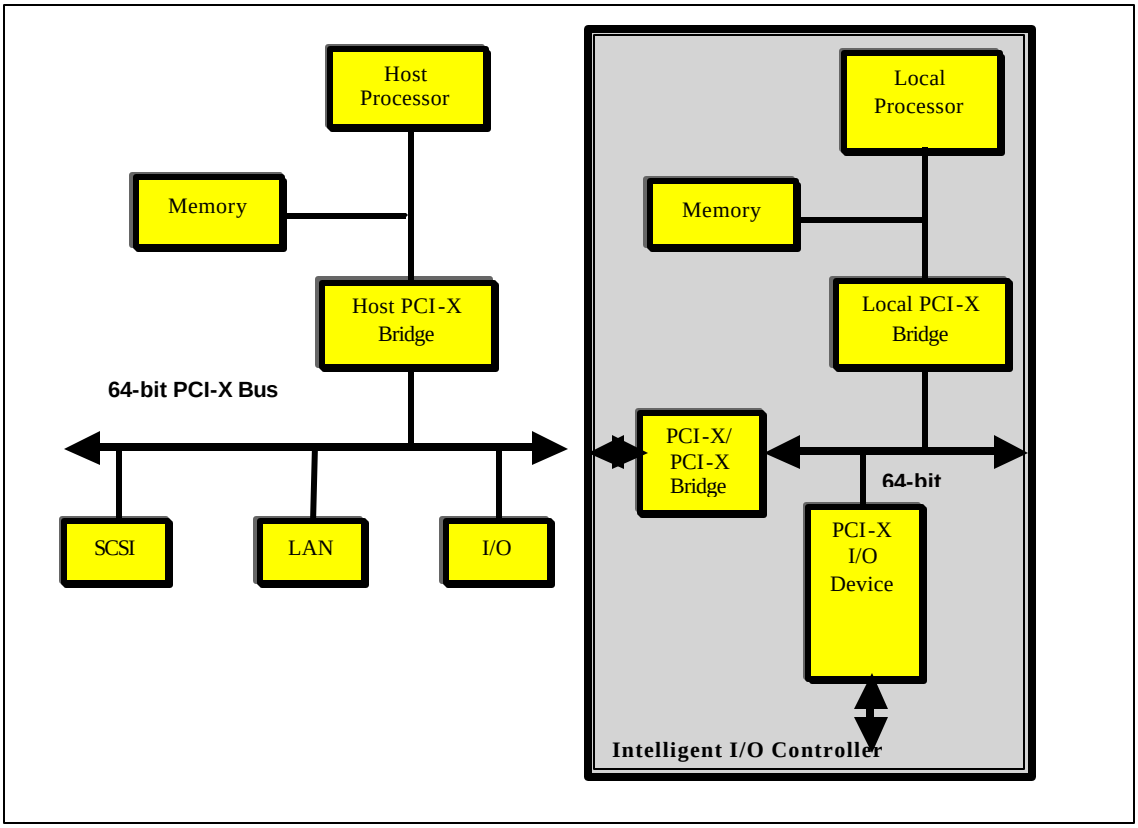

Figure 5: Typical Application – Intelligent I/O Controller

In Figure 5, a PCI-X-to-PCI-X bridge restricts the access of local resources from the host processor. By configuring the bridge as an embedded (non-transparent) bridge, the entire subsystem appears to be a single PCI-X/PCI device to the host. This type of functionality is useful in Compact PCI applications.

Summary

PCI-X provides a simple solution that bridges the increasing performance and bandwidth gap, which exists currently between the processors and the I/O, by increasing the attainable bandwidth at 133MHz. In addition, the slot capacity limitation at 66MHz for the conventional PCI has been eliminated by PCI-X as it supports 4 slots at 66MHz. There are additional benefits with this evolutionary I/O upgrade: it protects the customers' investment in hardware and software development; it provides a backward compatibility with the installed PCI-based systems; and it still leverages the PCI prevalence. Furthermore, there is strong industry support behind the PCI-X bus to ensure success of this open standard in achieving the goal of providing a simple, evolutionary path to a higher bandwidth I/O bus. There are various component and system level companies supporting the PCI-X enabling effort, including Compaq, IBM, HP, and Tundra Semiconductor. PCI-X helps to enable the network infrastructure to provide realistic information in real time to people.